REMARKS

The Examiner rejected claim 2 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written enablement requirement. The Examiner stated:

> "Claim 2, in lines 2 – 4, recites, ' . . . the phase locked-loop is operable to generate a plurality of clock signals that have a frequency higher than the frequency of the reference clock signal.' In the specification on page 8, as originally filed, the phase-locked loop receives a reference clock signal and generates a plurality of clock signals. There was no structure of circuit diagram to teach a person of ordinary skill in the art how the frequency of the plurality of clock signal is higher than the reference clock signal. Based on this, the specification fails to provide an enabling disclosure for claim."
> (typographical errors corrected)

The originally filed specification stated:

> "The phase-locked-loop 105 receives a reference clock signal 110 and generates a plurality of clock signals. Each of the plurality of clock signals has a frequency that is approximately equal to the frequency of the input data signal 115." page 2, lines 7 – 10.

Applicants believe that the phrase "approximately equal" includes both "higher than" and "lower than." However, to facilitate the prosecution of the patent application, Applicants have revised claim 2 to include the requirement that the "phase-locked-loop is operable to generate a plurality of clock signals that have a frequency approximately equal to the frequency of the reference clock signal."

The Examiner rejected claims 1 – 10 under 35 U.S.C. § 103(a) as being unpatentable over the prior art admitted by Applicants, Figure 2 of the patent application. In that regard, the Examiner stated:

> "The prior art differs from the claimed invention in that the prior art does not specifically disclose that the second latch-decision circuit is coupled to the clock-recovery circuit. However, as shown in the figure, the second latch-decision circuit is coupled to the second clock-recovery which is coupled to the second phase-locked loop which is further coupled to the clock-recovery circuit (220). Therefore, based on this, it would have been obvious, if it is not inherent, that the clock signal from the clock recovery circuit (220) is used to run the second phase-locked loop and the second latch-decision and hence coupling the clock recovery to the second latch-decision. One of ordinary skill in the art would

have been motivated to do this in order to synchronize timing of the system." (typographical errors corrected)

In an effort to clarify claim 1, Applicants have amended claim 1. Claim 1 now requires that the clock-recovery circuit generate a recovered clock signal. Claim 1 also requires that both the first latch-decision circuit and the second latch-decision circuit receive the recovered clock signal.

Applicants submit that claim 1 is not obvious in light of Figure 2 of the application ("the Prior Art"). The Examiner stated basis for modifying the Prior Art follows:

> "One of ordinary skill in the art would have been motivated to do this in order to synchronize timing of the system."

The purpose of the optical transmitter of claim 1 is not to "synchronize timing of the system." To the contrary, the purpose of the claimed optical transmitter is to allow for slightly unsynchronized input data signals. In high performance optical transmitters, completely synchronized latching is often not optimal. For example, one input data stream may travel a slightly different distance than another input data signal. Thus, the data signals are not exactly synchronized. Thus, simultaneous latching of the data signals is not optimal.

The Prior Art allows for slightly unsynchronized input data signals. More specifically, the Prior Art provides the flexibility of making latch decisions based on a recovered clock signal and the input data signal that is latched by the latch. Thus, an optical transmitter based upon the Prior Art can optimally latch a plurality of input data signals. However, while the Prior Art allows for slightly unsynchronized latching, the die size of the Prior Art optical transmitter is not minimized.

As is well known, the typical technique of minimizing die space of a multi-latch circuit is to utilize a single latch decision circuit to drive a plurality of latches. Using that technique, a single latch decision circuit would be utilized to latch a plurality of latches. If the purpose of the optical transmitter were to "synchronize timing of the system," as suggested by the Examiner, this conventional technique would be utilized. However, as discussed above, in high performance optical transmitters, such completely synchronized latching is not optimal.

The optical transmitter of claim 1 has the same flexibility as the Prior Art optical transmitter. In other words, latch decisions can be made based upon a recovered clock signal and

the input data signal that is latched by the latch. In addition, the optical transmitter of claim 1 has a minimized die size and a reduced cost compared to the Prior Art. Applicants submit that such a circuit is not obvious in light of the Prior Art.

From a structural perspective, the Prior Art does not include a clock recovery circuit that generates a recovered clock signal that is received by two latch-decision circuits. Instead, each latch-decision circuit in the Prior Art receives a separate and distinct recovered clock signal. As discussed above, modifying the Prior Art to the optical transmitter of claim 1 is not obvious.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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Date: January 25, 2005

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